

8

7

6

5

4

3

2

1

NOTES : UNLESS OTHERWISE SPECIFIED

1. DIMENSIONS ARE IN INCHES (EXCEPT WHERE NOTED).

ALL DOCUMENTS & SPECIFICATIONS REFERRED TO BELOW SHOULD BE THE LATEST REVISIONS.

MATERIAL : HOMOGENOUS MATERIALS IN THIS BOARD SHALL BE COMPLAINT WITH THE EU DIRECTIVE 2002/95/EC

2. BOARD MATERIAL:(USE CHECKED ITEMS)

(X) ISOLA 370HR OR SI000-2 OR IT180 OR EQUIVALENT

() ISOLA-FR408HR OR EQUIVALENT

() ISOLA IS410

() MEGTRON 6

() NELCO-4000-13

() ROGERS 4350B

() ROGERS 3003

() ARLON 85N

() EM370D

() OTHER _____

3. ALL LAMINATES & BONDING MATERIALS SHOULD BE SELECTED FROM IPC-4101 OR IPC-4103,(TG>170 DEGC TD>300 DEGC)

UL FLAMMABILITY RATING 94V-0. BOARD MATERIAL & CONSTRUCTION SHALL MEET THE REQUIREMENTS OF UL796/UL796F.

4. REFER TO IPC-6010 SERIES, CLASS 2 FOR FABRICATION. WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2.

5. REFER TO LAMINATION DIAGRAM FOR OVERALL BOARD THICKNESS, TOLERANCE APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES. FINISHED THICKNESS MEASURED FROM TOP COPPER TO BOTTOM COPPER.

6. BOW & TWIST NOT TO EXCEED 0.0075 INCHES (0.75%) PER LINEAR INCH AND SHOULD BE MEASURED PER IPC-TM-650, METHOD 2.4.22.

7. ACCEPTABILITY PER ADI SPECIFICATION TST00115.

TOOLING :

8. IMPEDANCE REQUIREMENTS: IF NO STACKUP IS DEFINED, THE VENDOR IS ALLOWED TO ADJUST THE DIELECTRIC THICKNESS & TRACE WIDTHS TO MEET THE IMPEDANCE REQUIREMENT. IF SPECIFIED, THE VENDOR MUST MEET THE REQUIREMENTS LISTED IN THE IMPEDANCE TABLE. ANY ADJUSTMENT MADE TO THE DEFINED STACKUP, TRACE WIDTH & SPACING THAT IMPACT THE REQUIREMENTS MUST HAVE WRITTEN APPROVAL FROM ADI.

9. FILLET OPTIONS TO ENHANCE RELIABILITY AT PAD JUNCTIONS WHERE SPACING PERMITS.

() FILLETS ALLOWED

(X) FILLETS NOT ALLOWED

10. THIEVING:

() VENDOR MAY ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS MAINTAINING A MINIMUM 0.100 INCH CLEARANCE FROM ALL COPPER FEATURES.

() VENDOR MAY NOT ADD THIEVING TO COMPENSATE FOR LOW COPPER DENSITY AREAS.

11. LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCHES.

FINISH :

12. DRILL SIZES ARE FINISHED HOLE SIZES. ALL HOLES SHALL BE LOCATED WITHIN 0.005 INCHES DTP,UNLESS SPECIFIED. MINIMUM BARREL PLATING OF 0.001 INCHES. PLATED HOLES SHALL NOT BE ROUGH OR IRREGULAR SO AS TO HINDER PROPER SOLDER WICKING. BARREL RELIEF ON SOLDERMASK ALLOWED IN UNFILLED VIA IN PAD HOLES.

13. PLATING SPECIFICATION:

(X) REFER TO LAMINATION DIAGRAM FOR FINISHED COPPER WEIGHT/THICKNESS REQUIRMENTS

THE STARTING COPPER WEIGHT/THICKNESS CAN VARY AS LONG AS THE FINISHED COPPER WEIGHT/THICKNESS IS NOT LESS THAN THE SPECIFIED VALUE.

14. SURFACE FINISH:

(X) IMMERSION GOLD (ENIG) 1.58-3.94 MICRO INCHES OVER 118-236 MICRO INCHES MIN. OF ELECTROLESS NICKEL PER IPC-4552

() OSP (ORGANIC SOLDERABILITY PRESERVATIVE)

() IMMERSION SILVER

() SOFT WIRE BONDABLE GOLD 30-50 MICRO INCHES OF SOFT WIRE

BONDABLE GOLD OVER 100-150 MICRO INCHES OF NICKEL

() EDGE CONNECTOR FINGERS ARE TO BE PLATED WITH 100 MICRO-INCHES(.0001") OF LOW STRESS NICKEL UNDER 30 MICRO-INCHES (.0003") OF GOLD

() OTHER_____

15. SOLDERMASK:

SOLDERMASK OVER BARE COPPER OR BARE GOLD (BOTH SIDES) TO MEET IPC-SM-840.

IF PRESENT,DO NOT MODIFY SOLDERMASK DEFINED PADS (MASK OPENINGS LESS THAN COPPER PAD) WITHOUT APPROVAL.

(X) LPI

() OTHER_____

COLOR

(X) GREEN

() OTHER_____

16. APPLY SILKSCREEN TO BOTH SIDES USING A NON-CONDUCTIVE, EPOXY BASED INK PER ARTWORK.

(X) WHITE

() OTHER

TESTING :

17. FINAL ELECTRICAL TEST TO BE PERFORMED USING PROVIDED IPC-D-356A NETLIST OR ODB++ FORMAT FILE. THE PCB SHALL HAVE A VERIFICATION STAMP.

18. A TIME DOMAIN REFLECTOMETER REPORT (TDR) FOR EACH IMPEDANCE CONTROLLED LAYER & A CERTIFICATE OF COMPLIANCE SHALL BE PROVIDED BY VENDOR AT TIME OF SHIPMENT. INSTANCES WHERE TDR TESTING CAN'T BE PERFORMED BECAUSE THE TRACE LENGTH IS TOO SHORT ON THE OUTER LAYERS AT THE PIN ESCAPES IS ACCEPTABLE. ALL OTHER INSTANCES MUST BE REPORTED.

MISCELLANEOUS :

19. IF PRESENT, ALL BLIND/BURIED VIAS WITH AN ASPECT RATIO <1:1 TO BE PLATED SHUT WITH COPPER WHEN USED AS VIA-IN-PAD OR AS A STACKED VIA. BLIND/BURIED VIAS WITH AN ASPECT RATIO >1:1 TO BE FILLED WITH NON-CONDUCTIVE EPOXY.

20. FOR VIA FILL INFORMATION REFER TO DRILL CHART:

() NON-CONDUCTIVE EPOXY FILL ALL 0.XXXX INCHES DRILLED VIAS

() COPPER FILL ALL 0.XXXX INCHES DRILLED VIAS

21. INTENTIONAL SHORTS:

IF AN INTENTIONAL SHORT REPORT IS SUPPLIED AND DOES NOT MATCH THE FAB DATA THEN ADI APPROVAL IS REQUIRED.

22. PEMNUTS:

() PEMNUTS TO BE INSTALLED BY FABRICATOR

() PEMNUTS NOT TO BE INSTALLED BY FABRICATOR

() NOT APPLICABLE

23. MANUFACTURER TO ETCH/STAMP WITH PERMANENT NON-CONDUCTIVE INK

ON SECONDARY SIDE UNLESS OTHERWISE SPECIFIED:

A. UL CODE-FLAMMABILITY RATING FOR THOSE APPROVED MATERIALS(IF APPLICABLE)

B. DATE CODE

C. LOT NUMBER

D. MANUFACTURER LOGO

24. SMOOTHEN EDGES AND FREE FROM BURRS AFTER DEPANELIZATION PROCESS

BOARDS TO BE SHIPPED SINGULATED AFTER FABRICATION PROCESS

25. MINIMUM DESIGN LINE WIDTH IS 0.030 INCH.

26. MINIMUM DESIGN LINE SPACING IS 0.0065 INCH.

FAB NOTES REVISION: 2ND NOVEMBER 2022

REV

DESCRIPTION

DATE

APPROVED

A

INITIAL RELEASE

09OCT23

D.CLAVILLAS

B

ECR-118582

22DEC23

D.CLAVILLAS

1.400IN

1.400IN

1.400IN

1.400IN

FINISHED HOLES IN MILS

ALL UNITS ARE IN MILS

FIGURE

SIZE

PLATED

QTY

TOLERANCE/NOTES

+

10.0

PLATED

180

DIA MAX

A

39.0

NON-PLATED

2

B

189.0

NON-PLATED

4

TOTAL HOLES: 186

IMPEDANCE TABLE (RFO ONLY)

IMPEDANCE TOLERANCE: +/-10%

LAYER

50 OHM

0 OHM

0 OHM

0 OHM

REFERENCE LAYER

TRACE WIDTH

TRACE WIDTH

TRACE WIDTH/SPACE

TRACE WIDTH/SPACE

TOP

0.033

-

-

-

BOTTOM

NOTE: DO NOT EDIT THIS TABLE MANUALLY;USE IMPEDANCE TABLE GENERATOR FROM ADI Tools.

LAMINATION DIAGRAM

LAYER NUMBER

LAYER NAME

COPPER THICKNESS (OZ,INCH)

DIELECTRIC THICKNESS (INCH)

MATERIALS

1 TOP

1 OZ, 0.0014" MIN

FINAL CU (THICKNESS AFTER PLATING)

2 BOTTOM

1 OZ, 0.0014" MIN

FINAL CU (THICKNESS AFTER PLATING)

THE FINISHED PCB THICKNESS TO BE: 0.062" +/-10%

PRIMARY SIDE

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN INCHES

TOLERANCES

DECIMALS FRACTIONS ANGLES

.XX .-. .010

.XXX .-. .005

.XXXX .-. .0050

-.1/32

-.2

APPROVAL

DATE

14APR21

14APR21

14APR21

TEMPLATE ENGINEER

BILLY PHILLIPS

HARDWARE SERVICES

BOB MACDONALD

HARDWARE SYSTEMS

DAVE WILLIAMS

TEST ENGINEER

N/A

COMPONENT ENGINEER

ADGT LIBRARY

TEST PROCESS

N/A

HARDWARE RELEASE

C. PASIA

22DEC23

GLOBAL OPERATIONS & TECHNOLOGY

804 WOBURN STREET

WILMINGTON, MA 01887

TITLE

FABRICATION

LTPOWER ANALYZER

INTERPOSER BOARD Z

FINISH

ENGINEER

D.CLAVILLAS

CHECKER

N/A

22DEC23

22DEC23

22DEC23

DO NOT SCALE DWG

SCALE

1/1

SHEET

1 OF 1

SIZE

FSCM NO

DRAWING NUMBER

REV

D

24355

09-080914

B